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Design and Analysis of Low Power Multimodulus Frequency Divider using True Single-Phase Clock (TSPC) and Extended-TSPC (ETSPC) Technologies

Dr. Antony P J
Professor & HoD, Department of Computer Science and Engineering,
A J Institute of Engineering &Technology, Mangaluru, India

Dr. Laxmi Gulappagol
Associate Professor, Department of Computer Science and Engineering,
A J Institute of Engineering &Technology, Mangaluru, India

Abstract

Frequency divider is an important element of transceivers in the application of wireless communication. The primary tool utilised in the development of frequency dividers is the phase locked loop (PLL). With a view of achieving the reduction in power consumption and attain high frequency of operation, PLLs are replaced with 2/3prescaler designs. This work proposes a dual modulus dual-modulus flexible divider with low power consumption that is implemented in 0.25um CMOS technology. The multimodulus divider consists of a proposed wideband multimodulus 32/33/47/48 prescaler, which is designed using True Single-Phase Clock (TSPC) and Extended-TSPC (ETSPC) technologies. The proposed system has maximum operating frequency of 5.2GHz for TSPC and 7.5GHz for ETSPC logics.

Keywords

Prescaler, multimodulus, TSPC , ETSPC.

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during the "5th International Conference on Recent Advancements in Engineering and Technology (ICRAET-2023)" organized by Institute For Engineering Research and Publication (IFERP) held on 19th & 20th May 2023, Bengaluru, India.

Mr. Siddth Kumar Chhajer
MD & Founder, IFERP
Technoarete Group

Mr. Rudra Bhanu Satpathy
CEO & Founder, IFERP
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